Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1.-57. (Canceled)

58. (new) A computing system, comprising:

a central processing unit;

a host memory coupled to said central processing unit, said host memory to store instructions executed by said central processing unit and data operated upon by way of said central processing unit executing said instructions;

a network interface to receive inbound IP packets and send outbound IP packets;

an offload processing subsystem, said offload processing subsystem communicatively coupled to said central processing unit and said network interface, said offload processing subsystem comprising:

a) TCP/IP logic circuitry for processing TCP/IP tasks on said inbound and outbound IP packets without using said central processing unit and said host memory;

b) SSL decryption logic circuitry for processing SSL tasks on said inbound IP packets without using said central processing unit and said host memory;

c) SSL encryption logic circuitry for processing SSL tasks on said outbound IP packets without using said central processing unit and said host memory;

d) a storage resource comprising one or more memory chips coupled to both said SSL decryption logic circuitry and said SSL encryption logic circuitry, said storage resource to store SSL processing information;

e) an offload memory coupled to said TCP/IP logic circuitry, said offload memory to store said inbound and outbound TCP/IP packets, said network interface coupled to said offload memory;

f) a first direct memory access (DMA) controller to retrieve said inbound IP packets from said offload memory, said first DMA controller coupled to said SSL decryption logic circuitry;

g) a second direct memory access (DMA) controller to retrieve said outbound IP packets from said host memory, said second DMA controller coupled to said SSL encryption logic circuitry;

59. (new) An computing system as in claim 58 wherein said inbound network interface comprises an Ethernet interface.

60. (new) The computing system as in claim 58 comprising a first buffer downstream from an output of said first DMA controller and upstream from an input of said SSL decryption logic circuitry, and, a second buffer downstream from an output of said second DMA controller and upstream from an input of said SSL encryption logic circuitry.